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# HD74HC273

Octal D-type Flip-Flops (with Clear)

# HITACHI

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## Description

This device contains 8 master-slave flip-flops with a common clock and common clear. Data on the D input having the specified setup and hold times is transferred to the Q output on the low to high transition of the clock input. The clear input when low, sets all outputs to a low state.

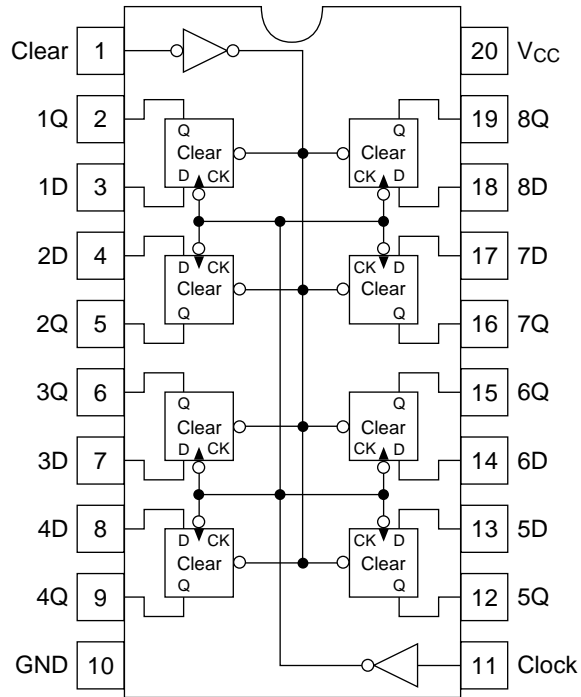
## Features

- High Speed Operation:  $t_{pd}$  (Clock to Q) = 18 ns typ ( $C_L = 50$  pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage:  $V_{CC} = 2$  to 6 V
- Low Input Current: 1  $\mu$ A max
- Low Quiescent Supply Current:  $I_{CC}$  (static) = 4  $\mu$ A max ( $T_a = 25^\circ\text{C}$ )

## Function Table

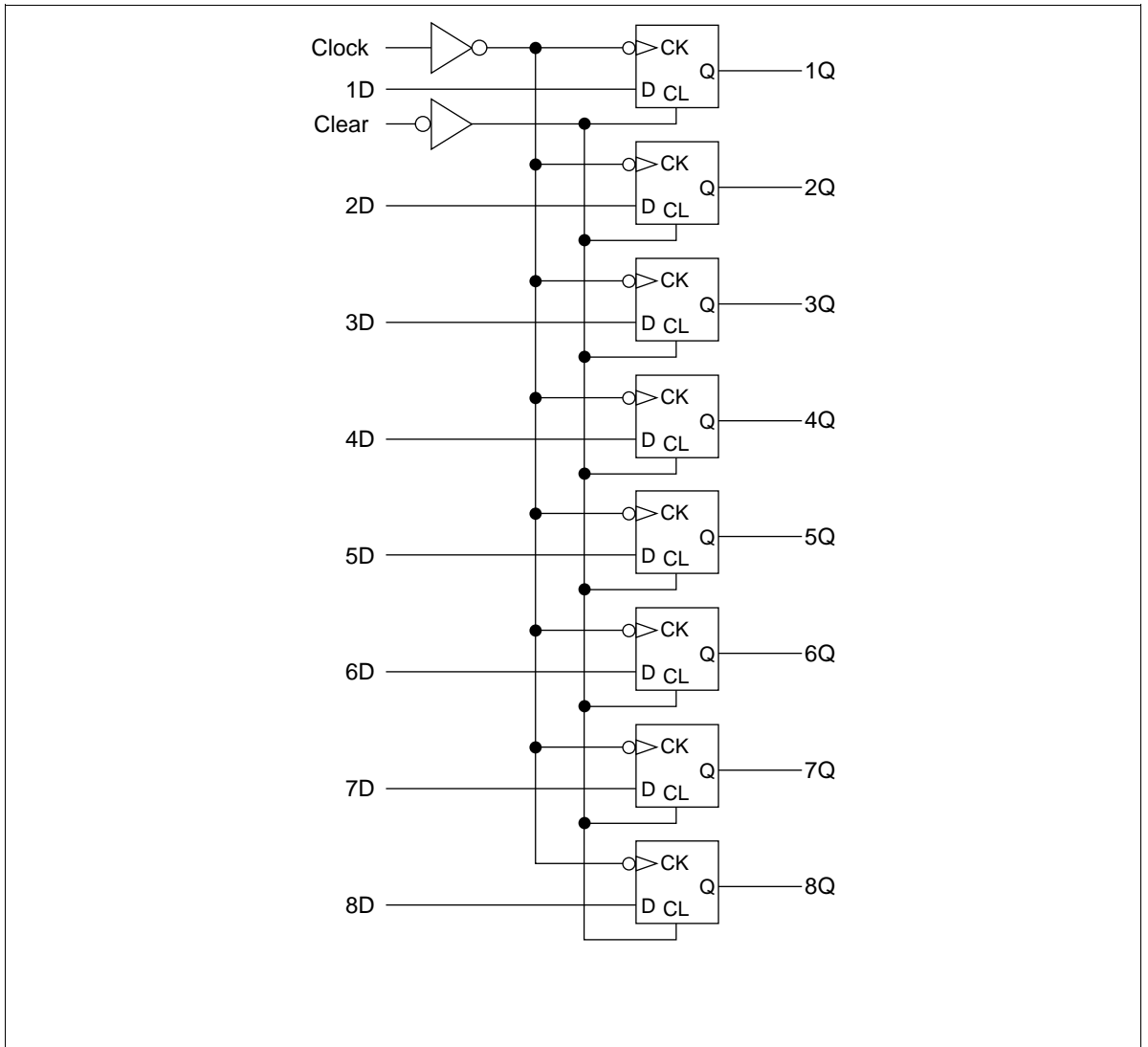
Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H		H	H
H		L	L
H	L	X	No change
H		X	No change

## Pin Arrangement



(Top view)

Logic Diagram

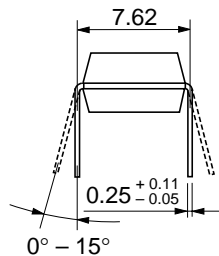
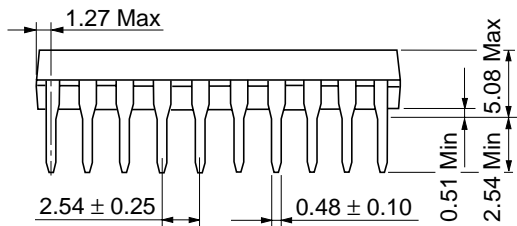
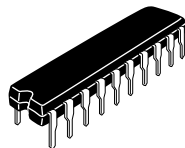
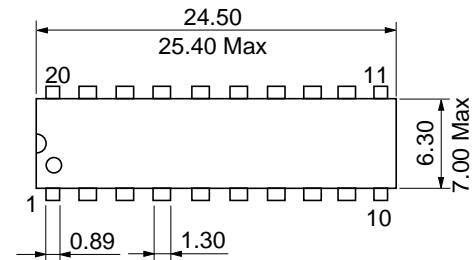


## DC Characteristics

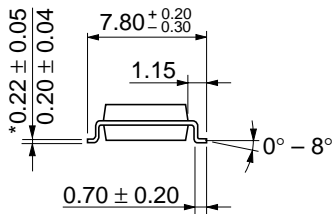
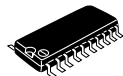
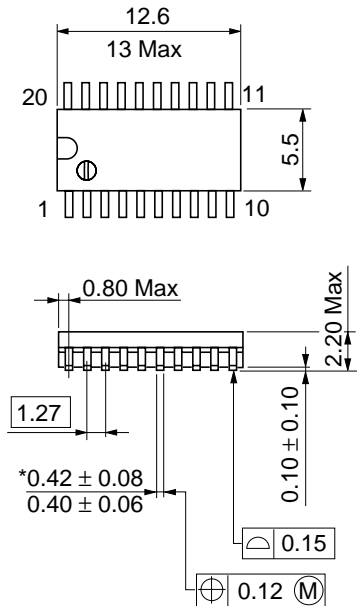
Item	Symbol	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V <sub>IH</sub>	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V <sub>IL</sub>	2.0	—	—	0.5	—	0.5			V
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V <sub>OH</sub>	2.0	1.9	2.0	—	1.9	—	V	Vin = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -20 μA	
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I <sub>OH</sub> = -4 mA
		6.0	5.68	—	—	5.63	—			I <sub>OH</sub> = -5.2 mA
	V <sub>OL</sub>	2.0	—	0.0	0.1	—	0.1	V	Vin = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 20 μA	
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I <sub>OL</sub> = 4 mA
		6.0	—	—	0.26	—	0.33			I <sub>OL</sub> = 5.2 mA
Input current	I <sub>in</sub>	6.0	—	—	±0.1	—	±1.0	μA	Vin = V <sub>CC</sub> or GND	
Quiescent supply current	I <sub>CC</sub>	6.0	—	—	4.0	—	40	μA	Vin = V <sub>CC</sub> or GND, I <sub>out</sub> = 0 μA	

AC Characteristics ( $C_L = 50 \text{ pF}$ , Input  $t_r = t_f = 6 \text{ ns}$ )

Item	Symbol	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	$f_{max}$	2.0	—	—	6	—	5	MHz	
		4.5	—	—	30	—	24		
		6.0	—	—	35	—	28		
Propagation delay time	$t_{PHL}$	2.0	—	—	145	—	180	ns	Clock to Q
		4.5	—	18	29	—	36		
		6.0	—	—	25	—	31		
	$t_{PLH}$	2.0	—	—	145	—	180	ns	
		4.5	—	18	29	—	36		
		6.0	—	—	25	—	31		
	$t_{PHL}$	2.0	—	—	145	—	180	ns	Clear to Q
		4.5	—	15	29	—	36		
		6.0	—	—	25	—	31		
Setup time	$t_{su}$	2.0	100	—	—	125	—	ns	Data to clock
		4.5	20	2	—	25	—		
		6.0	17	—	—	21	—		
Hold time	$t_h$	2.0	5	—	—	5	—	ns	Clock to data
		4.5	5	0	—	5	—		
		6.0	5	—	—	5	—		
Removal time	$t_{rem}$	2.0	100	—	—	125	—	ns	Clear to clock
		4.5	20	-1	—	25	—		
		6.0	17	—	—	21	—		
Pulse width	$t_w$	2.0	80	—	—	100	—	ns	Clock, clear
		4.5	16	8	—	20	—		
		6.0	14	—	—	17	—		
Output rise/fall time	$t_{TLH}$	2.0	—	—	75	—	95	ns	
	$t_{THL}$	4.5	—	5	15	—	19		
	$t_{THL}$	6.0	—	—	13	—	16		
Input capacitance	$C_{in}$	—	—	5	10	—	10	pF	

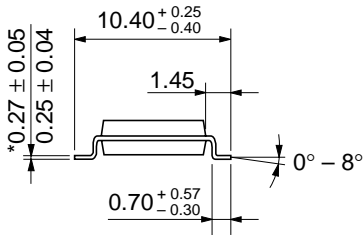
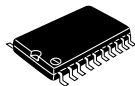
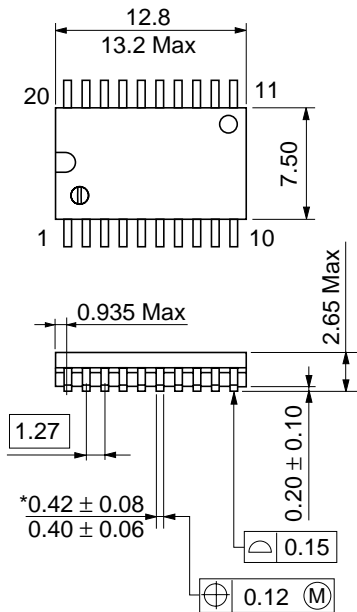


Hitachi Code	DP-20N
JEDEC	—
EIAJ	Conforms
Weight (reference value)	1.26 g



Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.31 g

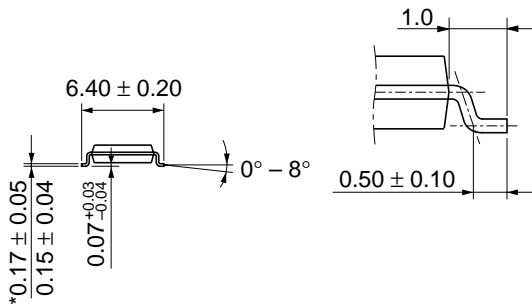
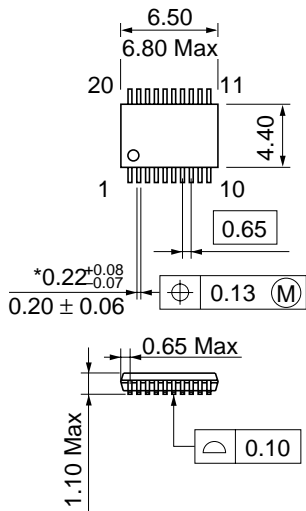
\*Dimension including the plating thickness  
Base material dimension



Hitachi Code	FP-20DB
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.52 g

\*Dimension including the plating thickness  
 Base material dimension





\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	TTP-20DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.07 g

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