SDLS107 - OCTOBER 1976 - REVISED MARCH 1988

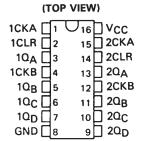
- Dual Versions of the Popular '90A, 'LS90 and '93A, 'LS93
- '390, 'LS390 . . . Individual Clocks for A and B Flip-Flops Provide Dual ÷ 2 and ÷ 5 Counters
- '393, 'LS393... Dual 4-Bit Binary Counter with Individual Clocks
- All Have Direct Clear for Each 4-Bit Counter
- Dual 4-Bit Versions Can Significantly Improve System Densities by Reducing Counter Package Count by 50%
- Typical Maximum Count Frequency . . . 35 MHz
- Buffered Outputs Reduce Possibility of Collector Commutation

description

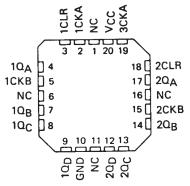
Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters in a single package. The '390 and 'LS390 incorporate dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a bi-quinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage. The '393 and 'LS393 each comprise two independent four-bit binary counters each having a clear and a clock input. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. The '390, 'LS390, '393, and 'LS393 have parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

Series 54 and Series 54LS circuits are characterized for operation over the full military temperature range of -55°C to 125°C; Series 74 and Series 74LS circuits are characterized for operation from 0°C to 70°C.

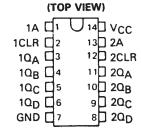
SN54390, SN54LS390 . . . J OR W PACKAGE SN74390 . . . N PACKAGE SN74LS390 . . . D OR N PACKAGE



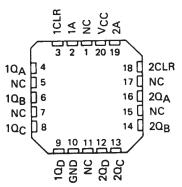
SN54LS390 . . . FK PACKAGE (TOP VIEW)



SN54393, SN54LS393 . . . J OR W PACKAGE SN74393 . . . N PACKAGE SN74LS393 . . . D OR N PACKAGE



SN54LS393 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection



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'390, 'LS390
BCD COUNT SEQUENCE
(EACH COUNTER)
(See Note A)

COUNT		συτ	PUT								
COONT	σ_{D}	σc	σ_{B}	QA							
0	L	L.	L	L							
1	L	L	L	н							
2	L	L	Н	ᆸ							
3	L	L	Н	н							
4	L	Н	L	ᅵ							
5	L	Н	L	н							
6	L	Н	Н	ᅵᅵ							
7	L	Н	Н	н							
8	н	L	L	L							
9	Н	L	L	Н							

FUNCTION TABLES
'390, 'LS390
BI-QUINARY (5-2)
(EACH COUNTER)
(See Note B)

COLUNIT		OUT	PUT	
COUNT	QΑ	a_{D}	α_{C}	$oldsymbol{Q}_{B}$
0	L	L	L	٦
1	L	L	L	н
2	L	L	Н	L
3	L	L	Н	н
4	L	Н	L	L
5	н	L	L	L
6	н	L	L	Н
7	н	L	Н	L
8	н	L	Н	н
9	Н	Н	L	L

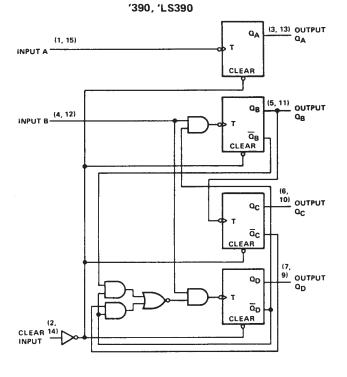
'393, 'LS393 COUNT SEQUENCE (EACH COUNTER)

COUNT		OUT	PUT	
CODIVI	a_{D}	αc	Q_{B}	QA
0	L	L	L	L
1	L	L	L	н
2	L	L	Н	L
3	L	L	Н	н
4	L	Н	L	L
5	L	Н	L	н
6	L	н	Н	L
7	L	Н	Н	-н
8	н	L	L	ᅵᅵ
9	н	L	L	н
10	н	L	н	L
11	н	L	Н	н
12	н	Н	L	L
13	н	Н	L	н
14	н	Н	Н	L
15	н	Н	Н	н

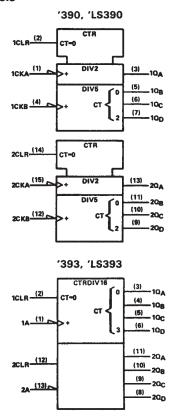
NOTES: A. Output QA is connected to input B for BCD count,

- B. Output Q_D^{\frown} is connected to input A for bi-quinary
 - count.
- C. H = high level, L = low level.

logic diagrams (positive logic)



logic symbols†

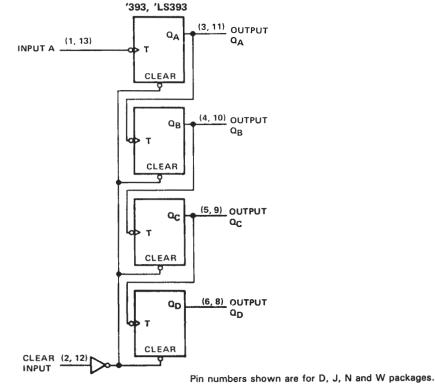


[†]These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

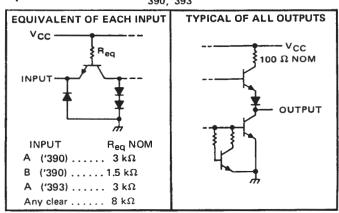




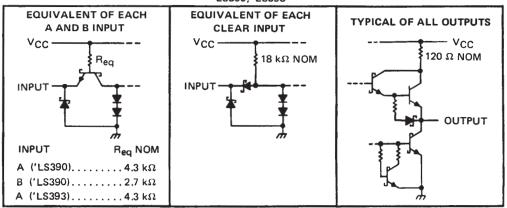


schematics of inputs and outputs

'390, '393



'LS390, 'LS393





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)	
Input voltage	
Operating free-air temperature range: SN54390, SN54393	
	0°C to 70°C
	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		- 1	SN54390 SN54393			SN74390 SN74393			
		MIN	NOM	MAX	MIN	NOM	MAX		
Supply voltage, V _{CC}		4.5	5	5.5	4.75	5	5.25	٧	
High-level output current, IOH				-800			-800	μΑ	
Low-level output current, IOL				16			16	mA	
Count francisco f	A input	0		25	0		25	MHz	
Count frequency, f _{count}	B input	0		20	0		20	IVIDZ	
	A input high or low	20			20				
Pulse width, t _W	B input high or low	25			25			ns	
	Clear high	20			20		•	1	
Clear inactive-state setup time, t _{su}	•	25↓			25↓			ns	
Operating free-air temperature, TA		-55		125	0		70	°C	

 $[\]downarrow$ The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	D		7507 00NF	NTIONO!		′390			′393		
	PARAMETER		TEST CONE	NI IONS.	MIN	TYP‡	MAX	MIN	TYP [‡]	MAX	UNIT
VIH	High-level input voltage				2			2			V
VIL	Low-level input voltage						0.8			0.8	V
VIK	Input clamp voltage		VCC = MIN, I	≖ –12 mA			-1.5			-1.5	V
Vон	High-level output voltage		V _{CC} = MIN, V V _{IL} = 0.8 V, I _C		2.4	3.4		2.4	3.4		V
VOL	Low-level output voltage		V _{CC} = MIN, V V _{IL} = 0.8 V, I _C	***		0.2	0.4		0.2	0.4	V
11	Input current at maximum input voltage		V _{CC} = MAX, V	j = 5.5 V			1			1	mA
		Clear	,				40			40	
ин	High-level input current	Input A	V _{CC} = MAX, V	j = 2.4 V			80			80	μΑ
		Input B					120				
		Clear					1			-1	
HL	Low-level input current	Input A	V _{CC} = MAX, V	j = 0.4 V			-3.2			-3.2	mA
		Input B					-4.8				
100	Short-circuit output current §		V-0 = MAY	SN54'	-20		57	-20		-57	mA
los	Short-circuit output current's		V _{CC} = MAX	SN74'	-18		-57	-18		-57	IIIA
Icc	Supply current		V _{CC} = MAX, Se	ee Note 2		42	69		38	64	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: ICC is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.



 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

[§] Not more than one output should be shorted at a time.

The QA outputs of the '390 are tested at IOL = 16 mA plus the limit value for IIL for the B input. This permits driving the B input while maintaining full fan-out capability.

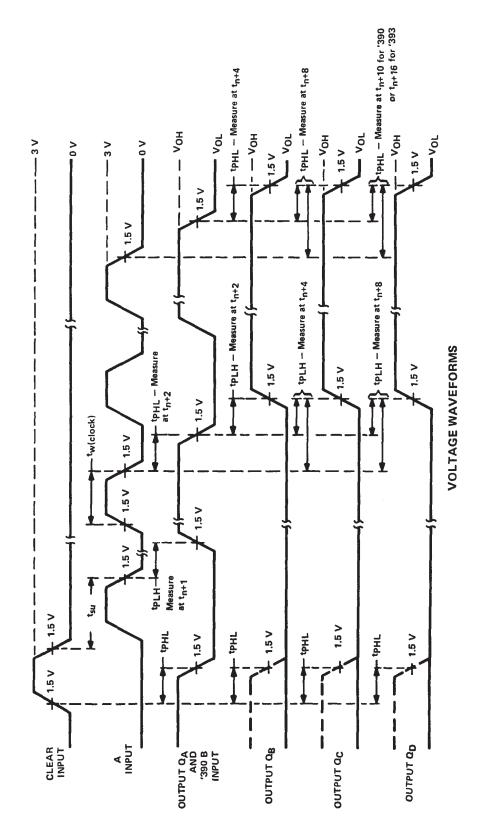
SDLS107 - OCTOBER 1976 - REVISED MARCH 1988

switching characteristics, VCC = 5 V, $T_A = 25^{\circ}C$

242445752	FROM	то	TEST CONDITIONS		′390			′393		UNIT
PARAMETER	(INPUT)	(OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	Civil
,	Α	QΑ		25	35		25	35		MHz
f _{max}	В	QB		20	30					141112
^t PLH	А	0	1		12	20		12	20	ns
tPHL		Q _A			13	20		13	20	1113
^t PLH		Q _C of '390	Cլ=15 pF,		37	60		40	60	ns
tPHL.	Α	Q _D of '393	R _L = 400 Ω,		39	60		40	60	1113
^t PLH	В	_	See Note 3		13	21				ns
t _{PHL}	В	QB	and		14	21				115
t _{PLH}	В	0 -	Figure 1		24	39				ns
[†] PHL	P	αc			26	39				113
^t PLH	В	0-]		13	21				ns
^t PHL	B	α_{D}			14	21				113
t _{PHL}	Clear	Any			24	39		24	39	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PARAMETER MEASUREMENT INFORMATION



NOTE A: Input pulses are supplied by a generator having the following characteristics t_r < 5 ns, t_f < 5 ns, PRR = 1 MHz, duty cycle = 50%, Z_{out} ≈ 50 ohms.

FIGURE 1



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)									 ٠.							. 7 V
Clear input voltage																
Any A or B clock input voltage									 							5.5 V
Operating free-air temperature range:	SN54	LS39	0, S	N54	LS39	3							-5	5°C	to	125°C
	SN74	LS39	0, S	N74	LS39	3								0°0	C to	70°C
Storage temperature range									 				-6	5°C	to	150°C
NOTE 1: Voltage values are with respect to netw																

recommended operating conditions

		_					N74LS390 N74LS393		
		MIN	NOM	MAX	MIN	NOM	MAX		
Supply voltage, V _{CC}		4.5	5	5.5	4.75	5	5.25	٧	
High-level output current, IOH				-400			-400	μΑ	
Low-level output current, IOL				4			8	mA	
0	A input	0		25	0		25	MHz	
Count frequency, f _{count}	B input	0		12.5	0		12.5	IVIFIZ	
	A input high or low	20			20				
Pulse width, tw	B input high or low	40			40			ns	
	Clear high	20			20			1	
Clear inactive-state setup time, t _{su}		25‡			25↓			ns	
Operating free-air temperature, TA		55		125	0		70	°C	

The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

							SN54L	S'	SN74LS'			UNIT
	PARAMETER		TES	T CONDITIONS		MIN	TYP‡	MAX	MIN	TYP‡	MAX	CIVIT
VIH	High-level input voltage					2			2			V
VIL	Low-level input voltage							0.7			0.8	V
VIK	Input clamp voltage		VCC = MIN,	I _I = -18 mA				-1.5			-1.5	V
Vон	High-level output voltage	1	V _{CC} = MIN, V _{IL} = V _{IL} max,	V _{IH} = 2 V, I _{OH} = -400 μA		2.5	3.4		2.7	3.4		V
.,			V _{CC} = MIN,	V _{IH} = 2 V,	IOL = 4 mA¶		0.25	0.4		0.25	0.4	V
VOL	Low-level output voltage		V _{IL} = 0.8 V,		IOL = 8 mA¶					0.35	0.5	
	Input ourroat at	Clear			V ₁ = 7 V			0.1			0.1	
Ц	Input current at maximum input voltage	Input A	V _{CC} = MAX		V ₁ = 5.5 V			0.2			0.2	mA
	maximum input vortage	Input B			V1 - 3.5 V			0.4			0.4	
		Clear						0.02	ļ		0.02	1
ΉΗ	High-level input current	Input A	$V_{CC} = MAX$,	$V_1 = 2.7 V$				0.1			0.1	mA
		Input B						0.2			0.2	
		Clear						-0.4			-0.4	1
1 ₁ L	Low-level input current	Input A	VCC = MAX,	V1 = 0.4 V				-1.6			-1.6	4
		Input B						-2.4			-2.4	<u> </u>
IOS	Short-circuit output curi	rent§	V _{CC} = MAX			-20		-100	-20		-100	
Lan	Supply ourrent		VCC = MAX,		'LS390		15	26		15		-l mA
Icc	Supply current		See Note 2		'LS393		15	26		15	26	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: I_{CC} is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.



 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

[§] Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

¹ The QA outputs of the LS390 are tested at IOL = MAX plus the limit value for IIL for the clock B input. This permits driving the clock B input while maintaining full fan-out capability.

SN54390, SN54LS390, SN54393, SN54LS393 SN74390, SN74LS390, SN74393, SN74LS393 DUAL 4-BIT DECADE AND BINARY COUNTERS SDLS107 - OCTOBER 1976 - REVISED MARCH 1988

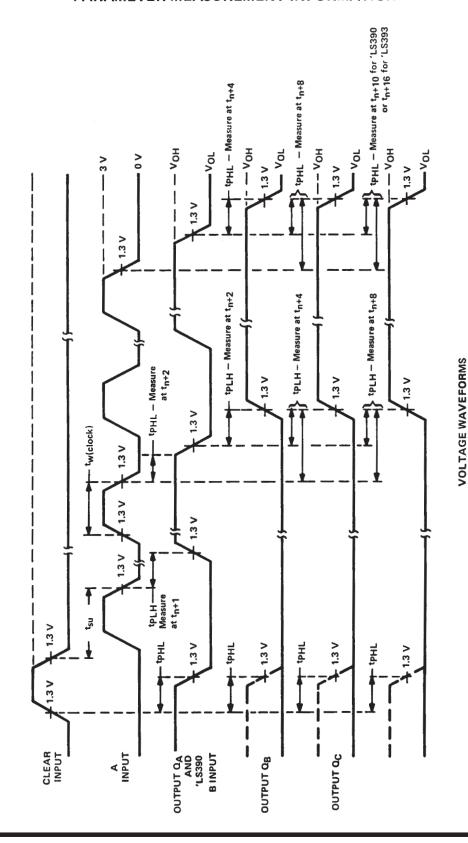
switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ} \text{ C}$

DADAMETED	FROM	то	7507 00MD1710M0		'LS390			'LS393		
PARAMETER	(INPUT)	(OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
	А	QA		25	35		25	35		MHz
f _{max}	В	QΒ]	12.5	20					IVITIZ
tPLH	A	0.			12	20		12	20	
^t PHL	7 ^	Q _A			13	20		13	20	ns
^t PLH	A	QC of 'LS390	C _L = 15 pF,		37	60		40	60	
^t PHL	1_^	Q _D of 'LS393	$R_{L} = 2 k\Omega$,		39	60		40	60	ns
^t PLH	В	0-	See Note 4 and Figure 2		13	21				
tPHL	1 -	QΒ			14	21				ns
tPLH .	В	0-			24	39				
tPHL.	1 6	σC			26	39				ns
^t PLH	В	0-			13	21				
^t PHL	1	σD			14	21				ns
tPH L	Clear	Any			24	39		24	39	ns

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.



PARAMETER MEASUREMENT INFORMATION



NOTE A: Input pulses are supplied by a generator having the following characteristics t₁< 15 ns, t₁< 6 ns, PRR = 1 MHz, duty cycle = 50 %,

 $Z_{out} \approx 50$ ohms.

FIGURE 2





PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp (3)
7802601EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
7802601FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
7802601FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
JM38510/32701B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/32701B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/32701BEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/32701BEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/32702B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/32702B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/32702BCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/32702BCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/32702BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
JM38510/32702BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
JM38510/32702SCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/32702SCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/32702SDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
JM38510/32702SDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SN54393J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN54393J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN54LS390J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS390J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS393J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS393J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN74390N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74390N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74393N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74393N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74393N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74393N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74LS390D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM





6-Dec-2006

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³
						no Sb/Br)		
SN74LS390N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS390N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS390N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS390N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS390NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS390NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS390NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIN
SN74LS393DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIN
SN74LS393J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN74LS393J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN74LS393N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS393N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS393N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74LS393N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74LS393NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS393NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS393NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIN
SN74LS393NSR	ACTIVE	SO	NS	14	2000	Green (RoHS &	CU NIPDAU	Level-1-260C-UNLIN





.com 6-Dec-2006

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp (3)
						no Sb/Br)		
SN74LS393NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54393J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SNJ54393J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SNJ54393W	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI
SNJ54393W	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI
SNJ54LS390FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS390FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS390J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS390J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS390W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS390W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS393FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS393FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS393J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS393J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS393W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SNJ54LS393W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE OPTION ADDENDUM

6-Dec-2006

www.ti.com	6-Dec-200
to Customer on an annual basis.	

14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB



W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC



FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AC.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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