

# SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244 SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SDLS144B – APRIL 1985 – REVISED FEBRUARY 2002

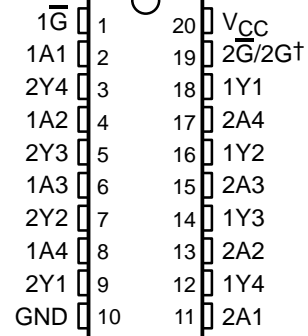
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- PNP Inputs Reduce DC Loading
- Hysteresis at Inputs Improves Noise Margins

## description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical, active-low output-control ( $\overline{G}$ ) inputs, and complementary output-control ( $G$  and  $\overline{G}$ ) inputs. These devices feature high fan-out, improved fan-in, and 400-mV noise margin. The SN74LS' and SN74S' devices can be used to drive terminated lines down to 133  $\Omega$ .

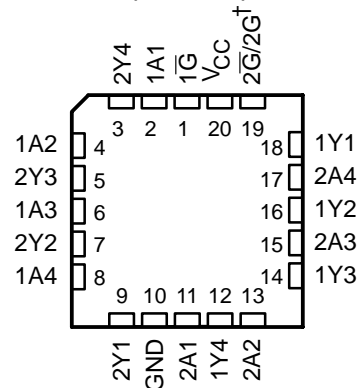
SN54LS', SN54S' . . . J OR W PACKAGE  
SN74LS240, SN74LS244 . . . DB, DW, N, OR NS PACKAGE  
SN74LS241 . . . DW, N, OR NS PACKAGE  
SN74S' . . . DW OR N PACKAGE

(TOP VIEW)



† 2G for 'LS241 and 'S241 or  $\overline{2G}$  for all other drivers.

SN54LS', SN54S' . . . FK PACKAGE  
(TOP VIEW)



† 2G for 'LS241 and 'S241 or  $\overline{2G}$  for all other drivers.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244  
 SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244  
 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS**

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**ORDERING INFORMATION**

<b>T<sub>A</sub></b>	<b>PACKAGE†</b>		<b>ORDERABLE PART NUMBER</b>	<b>TOP-SIDE MARKING</b>
0°C to 70°C	PDIP – N	Tube	SN74LS240N	SN74LS240N
			SN74LS241N	SN74LS241N
			SN74LS244N	SN74LS244N
			SN74S240N	SN74S240N
			SN74S241N	SN74S241N
			SN74S244N	SN74S244N
	SOIC – DW	Tube	SN74LS240DW	LS240
		Tape and reel	SN74LS240DWR	
		Tube	SN74LS241DW	LS241
		Tape and reel	SN74LS241DWR	
		Tube	SN74LS244DW	LS244
		Tape and reel	SN74LS244DWR	
		Tube	SN74S240DW	S240
		Tape and reel	SN74S240DWR	
		Tube	SN74S241DW	S241
		Tape and reel	SN74S241DWR	
		Tube	SN74S244DW	S244
		Tape and reel	SN74S244DWR	
	SOP – NS	Tube	SN74LS240NSR	74LS240
			SN74LS241NSR	74LS241
			SN74LS244NSR	74LS244
	SSOP – DB	Tape and reel	SN74LS240DBR	LS240
			SN74LS244DBR	LS244

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



**SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244  
SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244  
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS**

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**ORDERING INFORMATION (CONTINUED)**

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	CDIP – J	Tube	SN54LS240J	SN54LS240J
			SNJ54LS240J	SNJ54LS240J
			SN54LS241J	SN54LS241J
			SNJ54LS241J	SNJ54LS241J
			SN54LS244J	SN54LS244J
			SNJ54LS244J	SNJ54LS244J
			SN54S240J	SN54S240J
			SNJ54S240J	SNJ54S240J
			SN54S241J	SN54S241J
			SNJ54S241J	SNJ54S241J
			SN54S244J	SN54S244J
			SNJ54S244J	SNJ54S244J
	CFP – W	Tube	SNJ54LS240W	SNJ54LS240W
			SNJ54LS241W	SNJ54LS241W
			SNJ54LS244W	SNJ54LS244W
			SNJ54S240W	SNJ54S240W
			SNJ54S241W	SNJ54S241W
			SNJ54S244W	SNJ54S244W
	LCCC – FK	Tube	SNJ54LS240FK	SNJ54LS240FK
			SNJ54LS241FK	SNJ54LS241FK
			SNJ54LS244FK	SNJ54LS244FK
			SNJ54S240FK	SNJ54S240FK
			SNJ54S241FK	SNJ54S241FK
			SNJ54S244FK	SNJ54S244FK

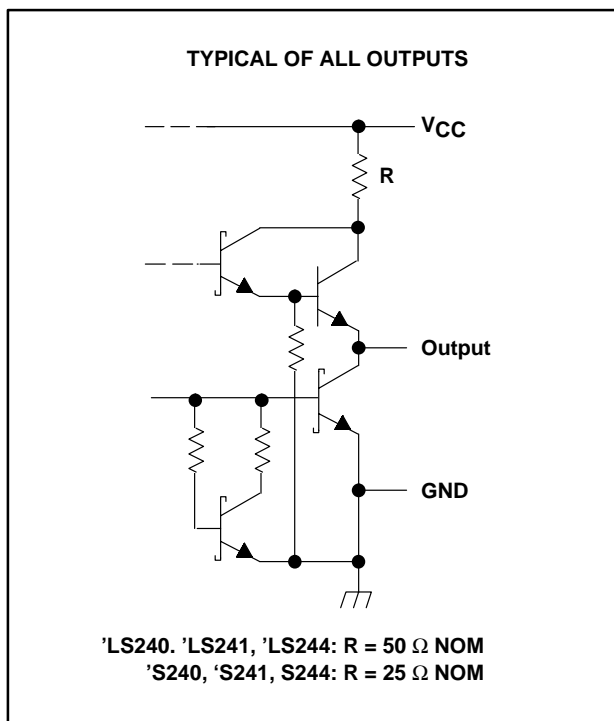
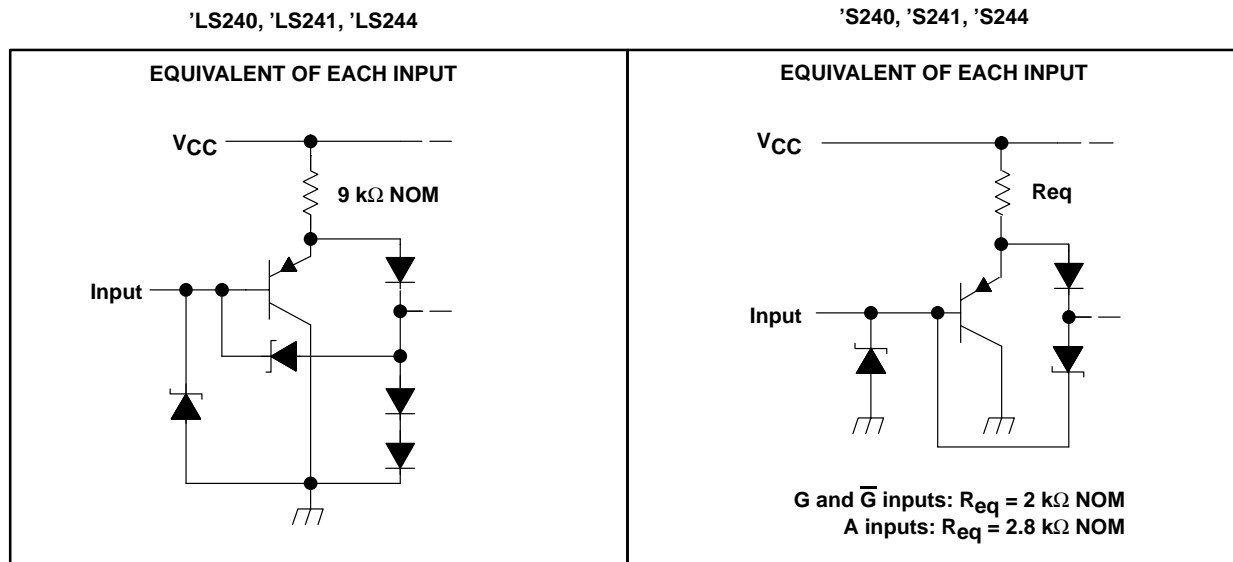
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



**SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244  
 SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244  
 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS**

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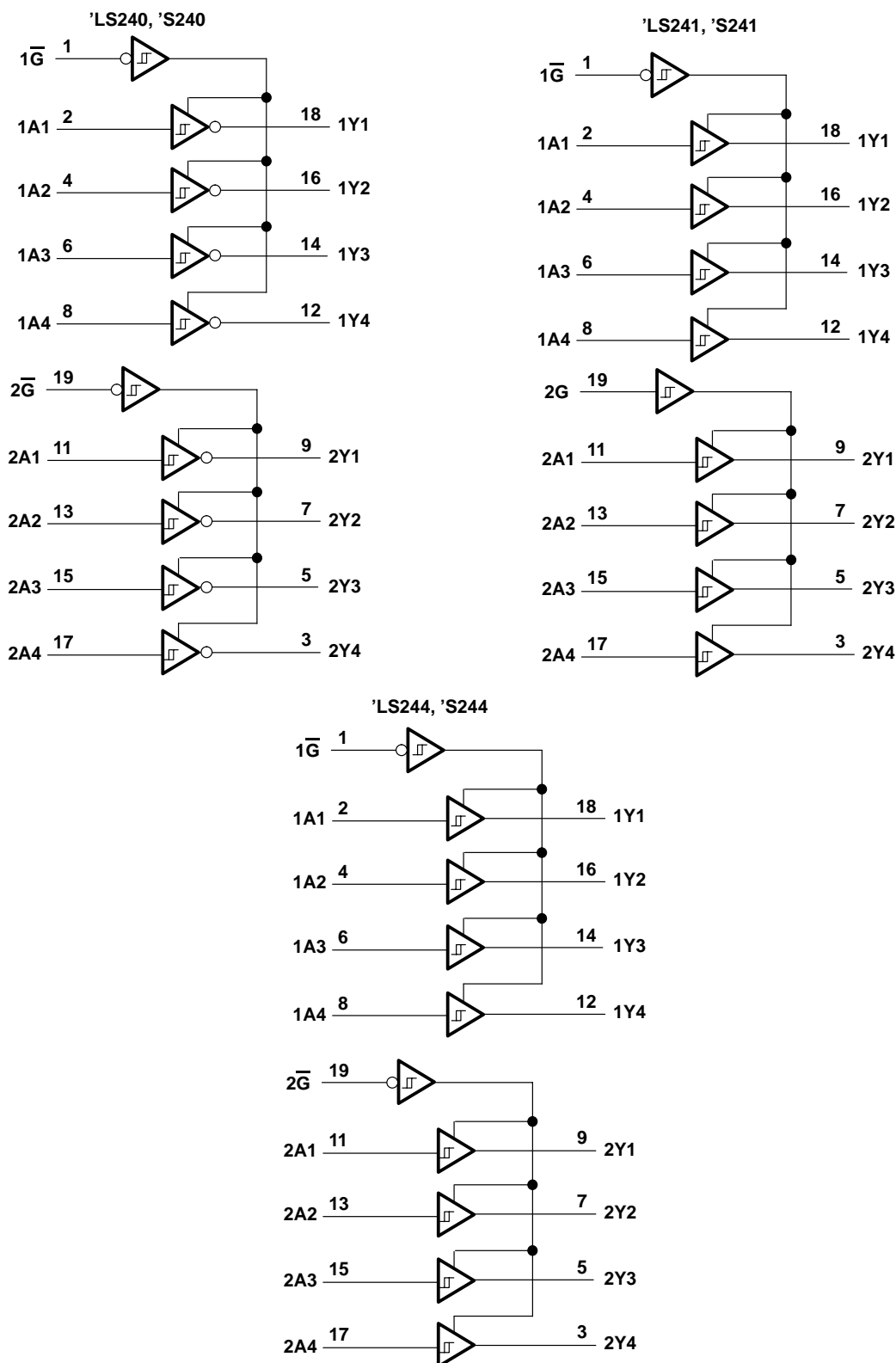
**schematics of inputs and outputs**



SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244  
 SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244  
 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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logic diagram



Pin numbers shown are for DB, DW, J, N, NS, and W packages.



**SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244  
 SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244  
 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS**

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage, $V_I$ : 'LS	7 V
'S	5.5 V
Off-state output voltage	5.5 V
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package	70°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Voltage values are with respect to network ground terminal.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions**

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage			0.7			0.8	V
$I_{OH}$ High-level output current			-12			-15	mA
$I_{OL}$ Low-level output current			12			24	mA
$T_A$ Operating free-air temperature	-55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.



**SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244  
SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244  
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS†		SN54LS'		SN74LS'		UNIT		
			MIN	TYP‡	MAX	MIN		TYP‡	MAX
V <sub>IK</sub>	V <sub>CC</sub> = MIN,	I <sub>I</sub> = -18 mA			-1.5		V		
Hysteresis (V <sub>T+</sub> - V <sub>T-</sub> )	V <sub>CC</sub> = MIN		0.2	0.4	0.2	0.4	V		
V <sub>OH</sub>	V <sub>CC</sub> = MIN, I <sub>OH</sub> = -3 mA	V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX,	2.4	3.4	2.4	3.4	V		
	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX	V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.5 V,	2		2				
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX	V <sub>IH</sub> = 2 V,	I <sub>OL</sub> = 12 mA			0.4	V		
			I <sub>OL</sub> = 24 mA			0.5			
I <sub>OZH</sub>	V <sub>CC</sub> = MAX, V <sub>IL</sub> = MAX	V <sub>IH</sub> = 2 V,	V <sub>O</sub> = 2.7 V			20	μA		
I <sub>OZL</sub>	V <sub>CC</sub> = MAX, V <sub>IL</sub> = MAX	V <sub>IH</sub> = 2 V,	V <sub>O</sub> = 0.4 V			-20	μA		
I <sub>I</sub>	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 7 V				0.1	mA		
I <sub>IH</sub>	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 2.7 V				20	μA		
I <sub>IL</sub>	V <sub>CC</sub> = MAX,	V <sub>IL</sub> = 0.4 V				-0.2	mA		
I <sub>OS</sub> §	V <sub>CC</sub> = MAX,					-40	-225	mA	
I <sub>CC</sub>	V <sub>CC</sub> = MAX, Output open	Outputs high	All		17	27	17	27	mA
		Outputs low	'LS240		26	44	26	44	
			'LS241, 'LS244		27	46	27	46	
		Outputs disabled	'LS240		29	50	29	50	
'LS241, 'LS244			32	54	32	54			

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see Figure 1)**

PARAMETER	TEST CONDITIONS		'LS240		'LS241, 'LS244		UNIT
			MIN	TYP	MAX	MIN	
t <sub>PLH</sub>	R <sub>L</sub> = 667 Ω,	C <sub>L</sub> = 45 pF	9	14	12	18	ns
t <sub>PHL</sub>			12	18	12	18	
t <sub>PZL</sub>	R <sub>L</sub> = 667 Ω,	C <sub>L</sub> = 45 pF	20	30	20	30	ns
t <sub>PZH</sub>			15	23	15	23	
t <sub>PLZ</sub>	R <sub>L</sub> = 667 Ω,	C <sub>L</sub> = 5 pF	10	20	10	20	ns
t <sub>PHZ</sub>			15	25	15	25	



# SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244 SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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## recommended operating conditions

		SN54S'			SN74S'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
I <sub>OH</sub>	High-level output current			-12			-15	mA
I <sub>OL</sub>	Low-level output current			48			64	mA
	External resistance between any input and V <sub>CC</sub> or ground			40			40	kΩ
T <sub>A</sub>	Operating free-air temperature (see Note 3)	-55		125	0		70	°C

NOTES: 1. Voltage values are with respect to network ground terminal.  
3. An SN54S241J operating at free-air temperature above 116°C requires a heat sink that provides a thermal resistance from case to free air, R<sub>θCA</sub>, of not more than 40°C/W.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONST		SN54S'			SN74S'			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN,	I <sub>I</sub> = -18 mA			-1.2			-1.2	V
Hysteresis (V <sub>T+</sub> - V <sub>T-</sub> )	V <sub>CC</sub> = MIN		0.2	0.4		0.2	0.4		V
V <sub>OH</sub>	V <sub>CC</sub> = MIN	V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -1 mA						2.7	V
	V <sub>CC</sub> = MIN,	V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -3 mA	2.4	3.4		2.4	3.4		
	V <sub>CC</sub> = MIN,	V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.5 V, I <sub>OH</sub> = MAX	2			2			
V <sub>OL</sub>	V <sub>CC</sub> = MIN,	V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = MAX			0.55			0.55	V
I <sub>OZH</sub>	V <sub>CC</sub> = MAX,	V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, V <sub>O</sub> = 2.4 V			50			50	μA
I <sub>OZL</sub>	V <sub>CC</sub> = MAX,	V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, V <sub>O</sub> = 0.5 V			-50			-50	μA
I <sub>I</sub>	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 5.5 V			1			1	mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 2.7 V			50			50	μA
I <sub>IL</sub>	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 0.5 V	Any A		-400	Any G		-400	μA
			Any G		-2	Any A		-2	mA
I <sub>OS</sub> §	V <sub>CC</sub> = MAX		-50		-225	-50		-225	mA
I <sub>CC</sub>	V <sub>CC</sub> = MAX, Output open	Outputs high	'S240	80	123	80	135	mA	
			'S241, 'S244	95	147	95	160		
		Outputs low	'S240	100	145	100	150		
			'S241, 'S244	120	170	120	180		
		Outputs disabled	'S240	100	145	100	150		
			'S241, 'S244	120	170	120	180		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.





**SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244  
 SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244  
 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS**

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switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (see Figure 2)

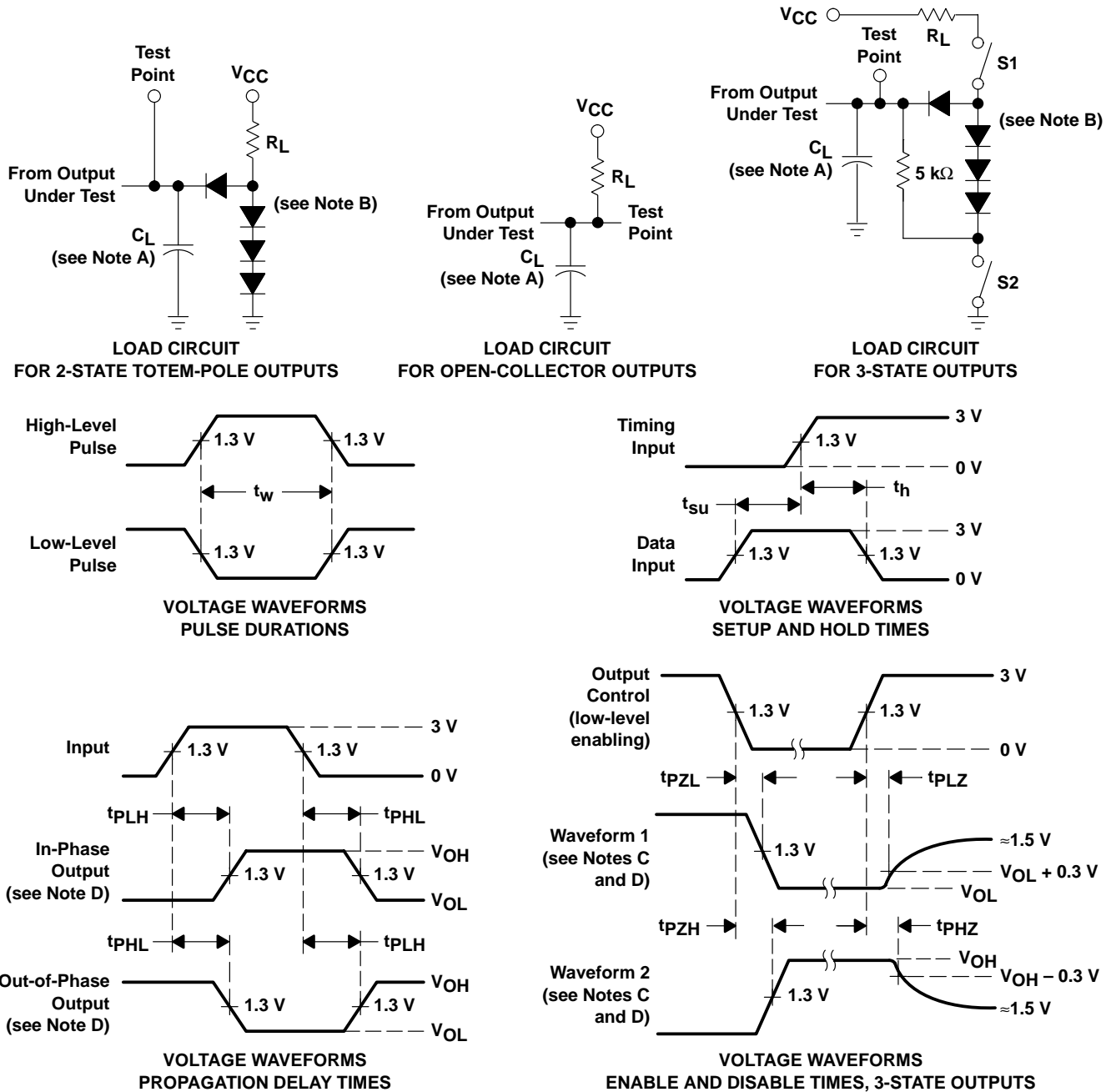
PARAMETER	TEST CONDITIONS	'S240			'S241, 'S244			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>PLH</sub>	R <sub>L</sub> = 90 Ω,      C <sub>L</sub> = 50 pF	4.5	7		6	9	ns	
t <sub>PHL</sub>		4.5	7		6	9		
t <sub>PZL</sub>	R <sub>L</sub> = 90 Ω,      C <sub>L</sub> = 50 pF	10	15		10	15	ns	
t <sub>PZH</sub>		6.5	10		8	12		
t <sub>PLZ</sub>	R <sub>L</sub> = 90 Ω,      C <sub>L</sub> = 5 pF	10	15		10	15	ns	
t <sub>PHZ</sub>		6	9		6	9		



**SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244  
SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244  
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS**

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**PARAMETER MEASUREMENT INFORMATION  
SERIES 54LS/74LS DEVICES**



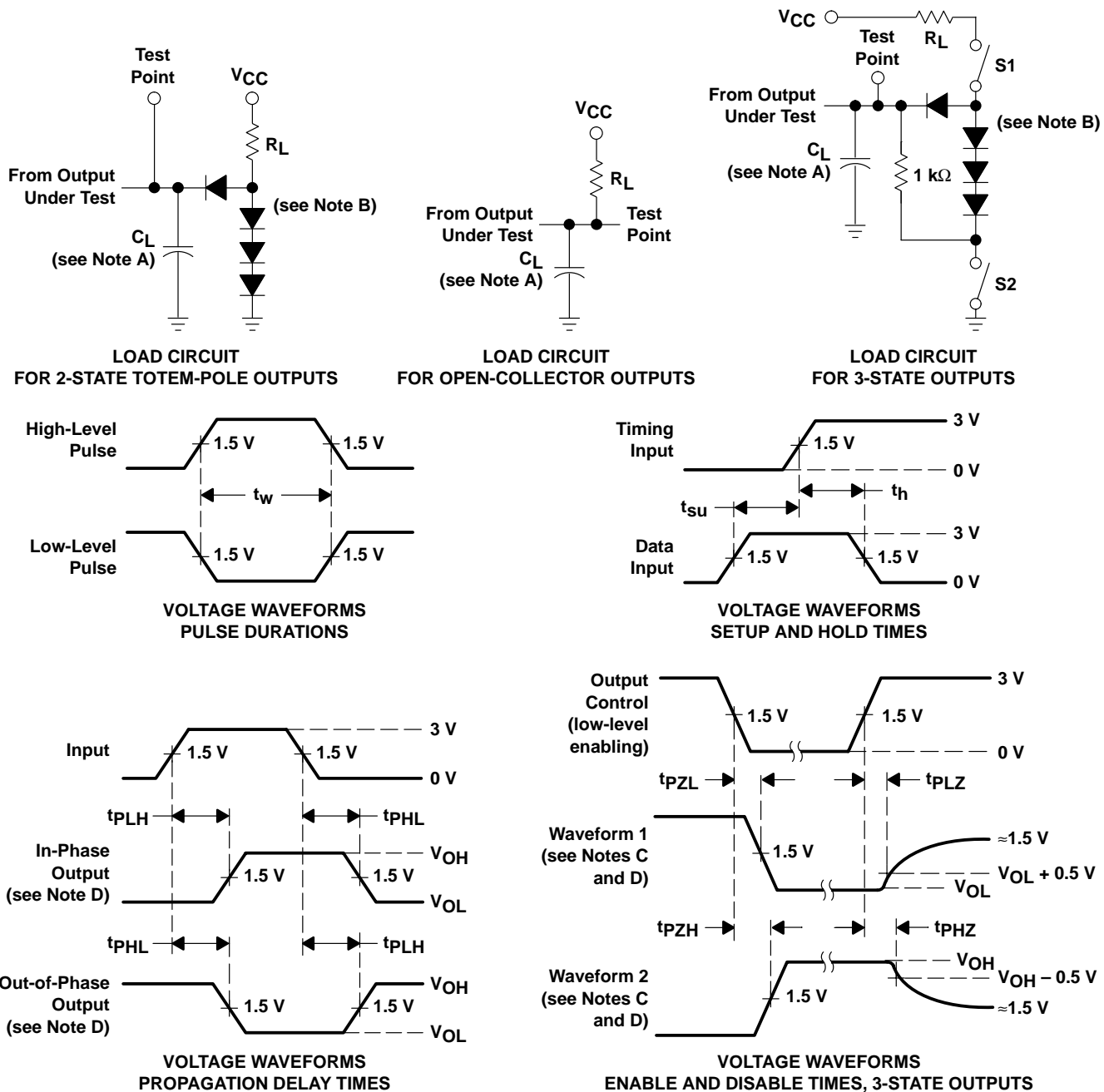
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All diodes are 1N3064 or equivalent.  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 D. S1 and S2 are closed for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_{PHZ}$ , and  $t_{PLZ}$ ; S1 is open and S2 is closed for  $t_{PZH}$ ; S1 is closed and S2 is open for  $t_{PZL}$ .  
 E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.  
 F. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O \approx 50 \Omega$ ,  $t_r \leq 15$  ns,  $t_f \leq 6$  ns.  
 G. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244  
 SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244  
 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION  
 SERIES 54S/74S DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All diodes are 1N3064 or equivalent.  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 D. S1 and S2 are closed for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_{PHZ}$ , and  $t_{PLZ}$ ; S1 is open and S2 is closed for  $t_{PZH}$ ; S1 is closed and S2 is open for  $t_{PZL}$ .  
 E. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O \approx 50 \Omega$ ;  $t_r$  and  $t_f \leq 7$  ns for Series 54/74 devices and  $t_r$  and  $t_f \leq 2.5$  ns for Series 54S/74S devices.  
 F. The outputs are measured one at a time with one input transition per measurement.

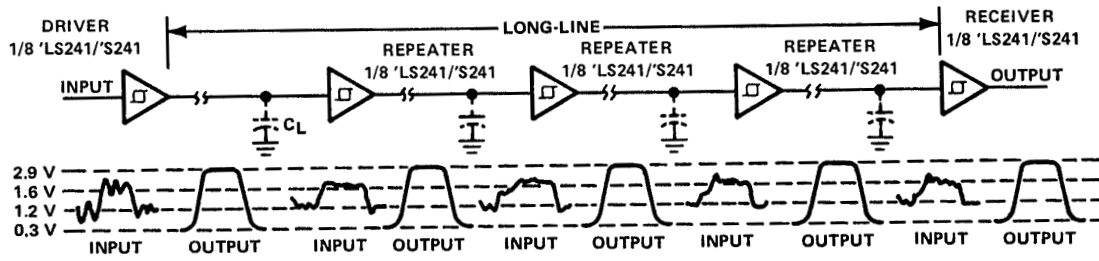
Figure 2. Load Circuits and Voltage Waveforms



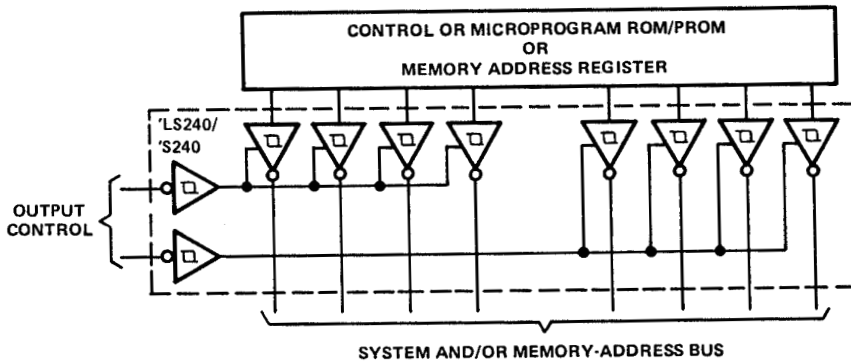
# SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244 SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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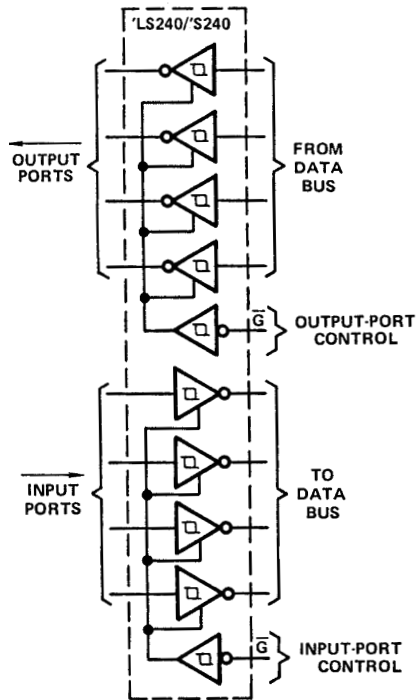
## APPLICATION INFORMATION



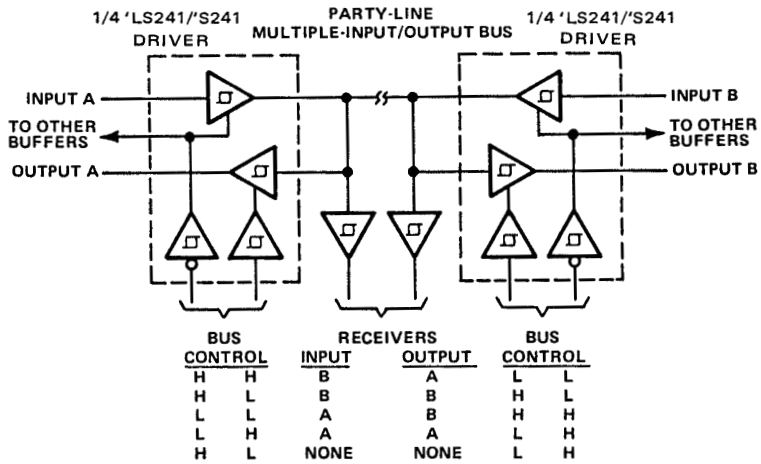
'LS241, 'S241 USED AS REPEATER/LEVEL RESTORER



'LS240/'S240 USED AS SYSTEM AND/OR MEMORY BUS DRIVER—4-BIT ORGANIZATION CAN BE APPLIED TO HANDLE BINARY OR BCD



INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS IN A SINGLE PACKAGE



PARTY-LINE BUS SYSTEM WITH MULTIPLE INPUTS, OUTPUTS, AND RECEIVERS

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-7801201VRA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
5962-7801201VSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type
7705701RA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
7705701SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type
78012012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
7801201RA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
7801201SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type
JM38510/32401B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/32401BRA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/32401BSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type
JM38510/32402B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/32402BRA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/32402BSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type
JM38510/32403B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/32403BRA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/32403BSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type
JM38510/32403SRA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/32403SSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type
SN54LS240J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS241J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS244J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SN54S240J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SN54S241J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SN54S244J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SN74LS240DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS240DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS240DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS240J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI
SN74LS240N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS240N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74LS240NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS240NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS240NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS240NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS241DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS241DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
						no Sb/Br)		
SN74LS241DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS241DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS241J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI
SN74LS241N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS241N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74LS241NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS241NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS241NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS244DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS244DBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS244DBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS244DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS244DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS244DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS244DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS244DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS244DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS244J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI
SN74LS244N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS244N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74LS244NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS244NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS244NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS244NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S240DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S240DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S240DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74S240DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S240N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74S240N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74S240NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74S241DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S241DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S241DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S241DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S241J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI
SN74S241N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74S241N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74S241NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74S244DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S244DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S244DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S244DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S244J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI
SN74S244N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74S244N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74S244NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SNJ54LS240FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS240J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS240W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type
SNJ54LS241FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS241J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS241W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type
SNJ54LS244FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS244J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS244W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type
SNJ54S240FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54S240J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54S240W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type
SNJ54S241FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SNJ54S241J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54S241W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type
SNJ54S244FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54S244J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54S244W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

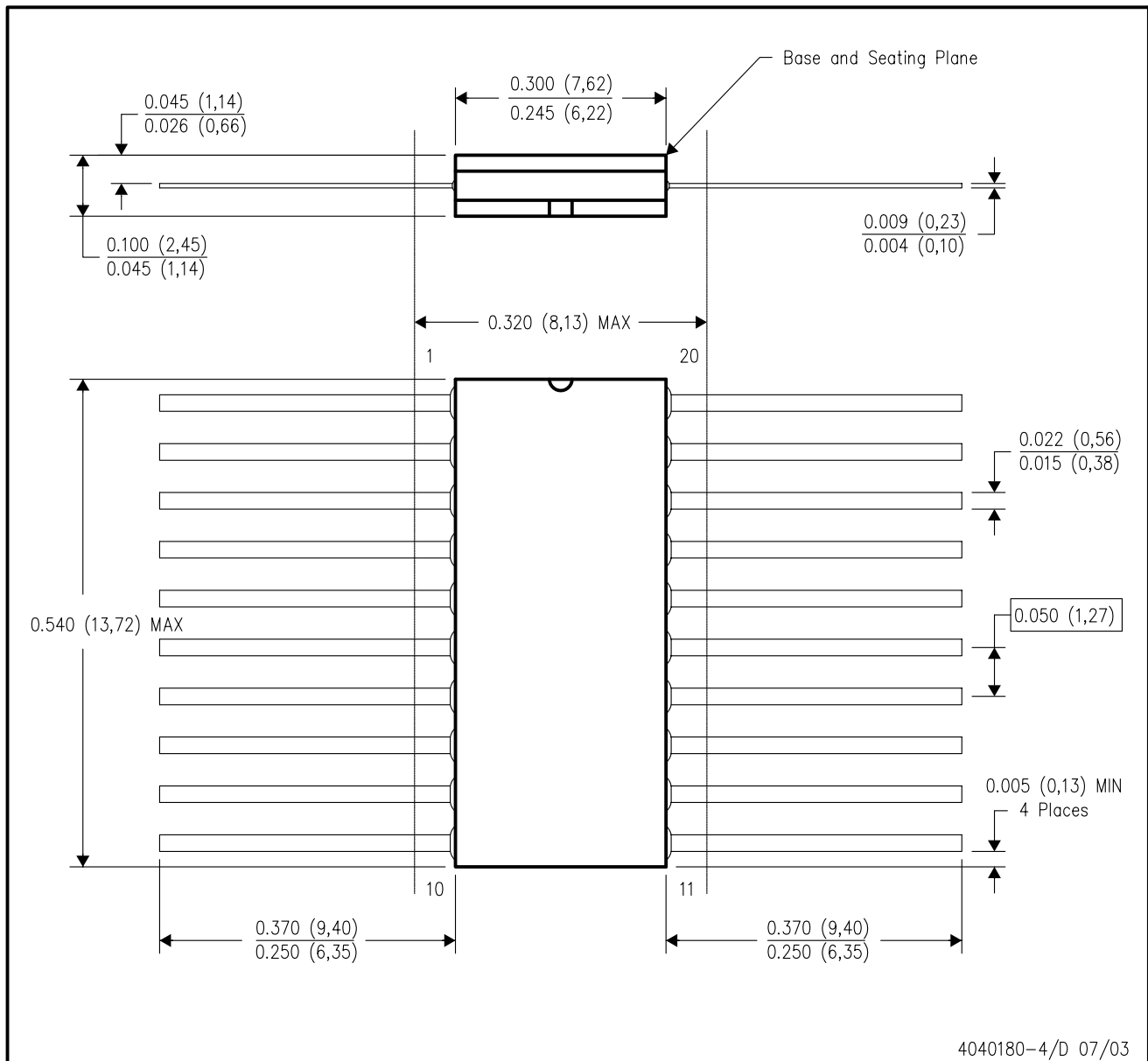


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

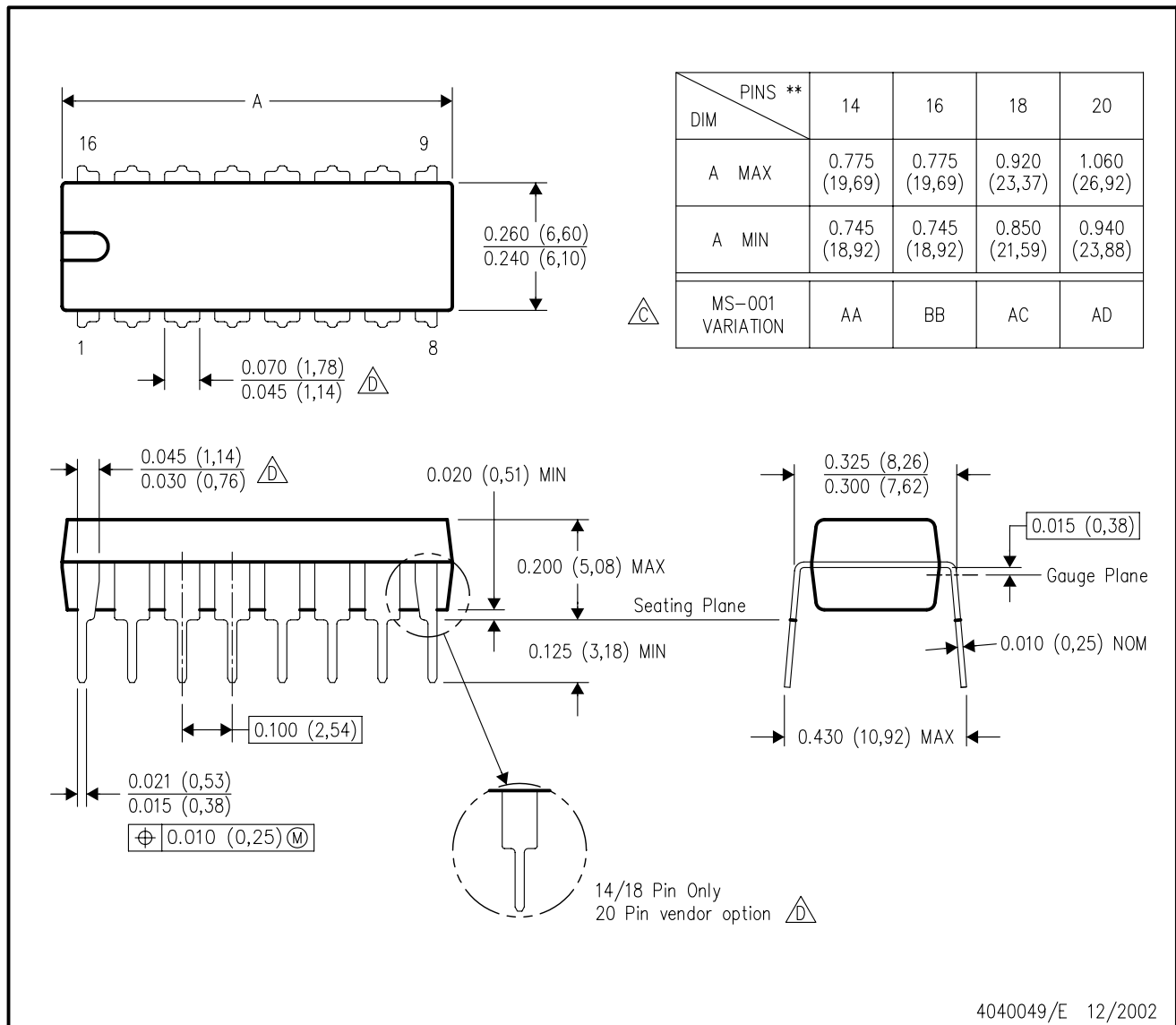


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

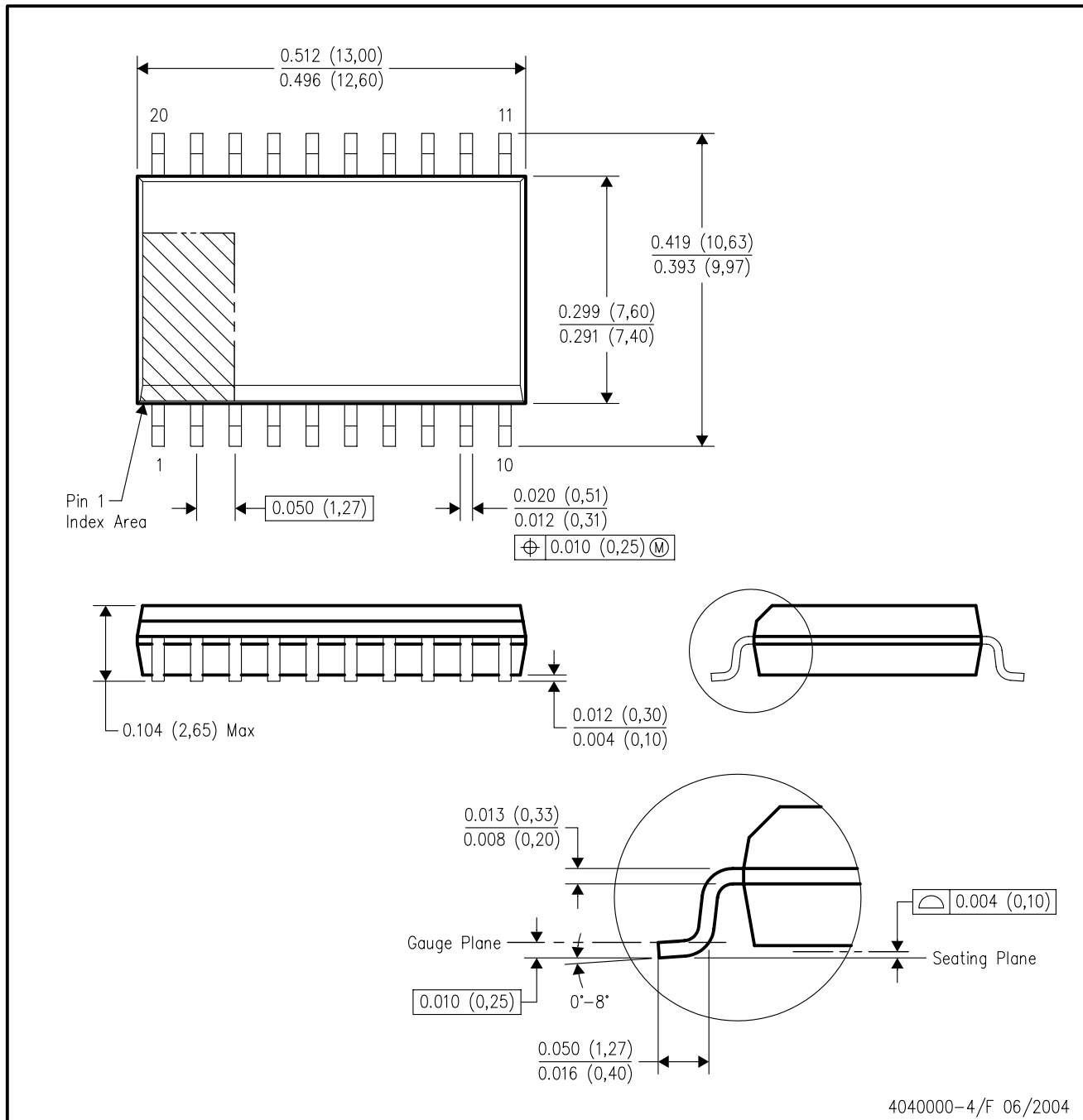
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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Low Power Wireless	<a href="http://www.ti.com/lpw">www.ti.com/lpw</a>	Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
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